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ESB: A low-cost EEG Synchronization Box

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ABSTRACT

Electroencephalography (EEG) is a neuroimaging technique with a temporal resolution in the millisecond scale. Popular ERPs and ERD/ERS functions, as well as EEG-fRMI data and hyperscanning methods requires a proper temporal alignment (namely, synchronization) with stimulus onsets and other devices. Hardware-based synchronization, based on a SYNC signal injected into the device, ensures a reliable timing. In this paper we describe the design, test and validation of an EEG Synchronization Box (ESB), able to condition and distribute a SYNC signal (analog and digital) to different devices simultaneously. ESB can be easily built by individuals with basic soldering skills and represents a cost-effective solution to the available commercial synchronization boxes, while preserving similar electrical and functional features.

1. Specifications table:

Hardware name	ESB - EEG Synchronization Box
Subject area	• Biomedical Engineering • Electrical and Electronics Engineering • Neuroscience
Hardware type	• Trigger circuit • synchronization circuit
Open source license	GNU General Public License (GPL) 2.0
Cost of hardware	~35.00€
Source file repository	https://osf.io/ctkmh https://github.com/mbilucaglia/ESB

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2. Hardware in context

Functional Neuroimaging aims to measure the brain activity associated with cognitive, emotional and motor processes. Nowadays, several modalities, such as Positron Emission Tomography (PET), Functional Magnetic Resonance Imaging (fMRI) and Electroencephalography (EEG), are available. Apart for their underlying physical principles, they differ for resolution, both spatial (i.e. the ability to distinguish activity changes across different spatial locations) and temporal (i.e. the ability to separate brain events in time) [1].

The EEG is a measure of the difference of electric potential between couples of electrodes placed on the scalp. Scalp potentials are believed to reflect the averaged synaptic activity of large neural volumes, consisting in about 10^8 to 10^9 neurons from the outer layer of the cortex [2]. Despite its poor spatial resolution, EEG proves a very high temporal resolution, within the millisecond scale [3].

EEG is widely used in clinical ad experimental neuroscience. Popular examples are the Event-Related Potentials (ERPs) [4] and the Event-Related Desinchronization/Event-Related Synchronization (ERD/ERS) [5] functions that represent brain changes phase-locked and time-locked to stimuli or events. Additionally, EEG is often simultaneously recorded with fMRI, in order to produce spatiotemporally resolved EEG-fMRI images [6]. Finally, the so-called hyperscanning methods, namely multiple temporally-synchronized EEG recordings, are becoming popular to study the brain changes during social and cooperative tasks [7].

All the above mentioned examples require a proper temporal alignment (namely, synchronization) of the EEG data, both with the event/stimulus onsets [4] and with the fMRI data [8], as well as among multiple EEG devices [9]. The synchronization can following either a hardware or a software-based strategy [10,11].

Hardware synchronization is based on a proper synchronization signal (hereinafter, SYNC) injected into a dedicated digital port, usually available on high-end commercial EEG devices [12]. When not available, the SYNC can be recorded from either a dedicated input channel (e.g. bipolar AUX channel) or a couple of standard EEG channels, after being eventually attenuated and optoisolated [13]. The SYNC is typically a pulse-like aperiodic signal, generated by either the serial/parallel PC port or by sensors (e.g. photodetectors, response buttons, microphones) and serves to mark various events-of-interests. Depending from the situation, the events-of-interests can be the stimulus/event onsets (ERP and ERD/ERS) or the start of the recording/scanning (EEG-fMRI and hyperscanning methods).

Software synchronization is based on a recording/integrating application running on a computer, such as the open source LSL (Lab Streaming Layer) framework [14]. LSL synchronization is based on the alignment of the timestamps, which are collected alongside with each actual sample data and each presented event [11]. It is clear that the selected EEG device must be supported by the PC application, either with a dedicated driver or through an available API (Application Programming Interface).

Unfortunately, most of the available recording/integrating applications do not support low cost devices and only hardware synchronization is possible. Even when fully supported by PC applications, low cost devices often suffer of severe jitter and hardware synchronizations represent the only reliable solution [12]. Despite the fact LSL can achieve a millisecond precision or better [14], hardware synchronization is still considered the best synchronization strategy [15], considering that alignment differences, ranging from 12.1% to 15.9%, have been reported in a recent comparative analysis [16].

In this paper we describe the design, test and validation of a EEG Synchronization Box (namely, ESB) able to condition and distribute a SYNC to different devices simultaneously, performing an hardware-based synchronization with potentially any type of EEG device, either equipped with a dedicated digital/analog channel or not. Additional goals included the wide input voltage range, making it compatible to different type of input SYNC signals (e.g. analog and digital), as well as a low price and ease of assembly. During the design we followed the electrical and functional features of pre-existing commercial synchronization boxes, (summarized in Table 1): the StimTrack by Brain Products (https://www.brainproducts.com/productdetails.php?id=57) and the g.TRIGBOX by g.TEC (https://www.gtec.at/product/gtrigbox/). The functional diagram of the ESB is shown in Fig. 1.

Table 1
Main features of some pre-existing commercial synchronization boxes.

	StimTrack (Brain Products)	g.TRIGbox (g.TEC)
Input voltage	±5 V	±0.5 mV ±200 mV ±100 mV ±5 V
Treshold voltage	adjustable	adjustable
Output voltage	±5 V (analog) 0–5 V (TTL)	0–200 mV (analog) 0–5 V (TTL)
Galvanic isolation	1.5 kV	4 kV
Trigger modality	1 High	1 High
Minimun pulse in duration	10 µs	N/A
Minimum pulse out duration	11 ms	20 ms
#Inputs	1	4
#Outputs	1	4
Indicative price	1300.00 €	2900.00 €

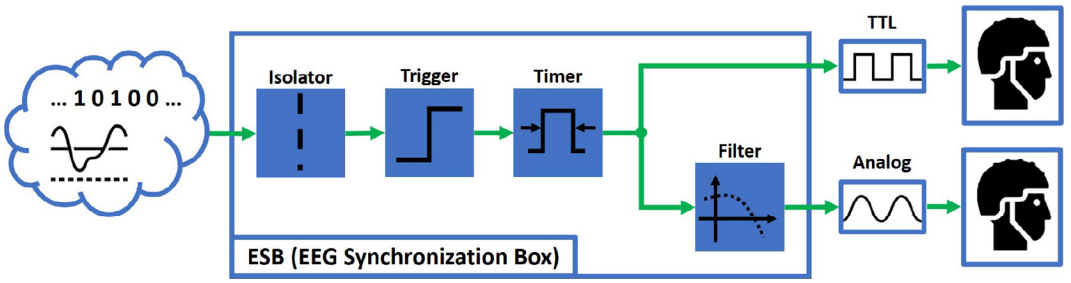

Fig. 1. Functional diagram of the ESB.

3. Hardware description

Electrical safety is a critical aspect in medical instrumentation design. Because of their finite impedance, a nonzero electrical current can flow across the human tissues after the application of a nonzero external voltage. Depending on the intensity, frequency and stimulation duration, as well as the locations of the points of entry, the electrical current flow produces various biological effects, ranging from perception and muscles paralysis to tissue injuries and ventricular fibrillation (the so-called electric shock). Thanks to the skin impedance (in the 15–1000 $k\Omega/cm^2$ range), when the entry points are located on the body surface, the voltage required to produce an electric shock (called *macroshock*) is increased. Macroshocks can be avoided by either powering the device with low voltage (<10 V) batteries or isolating any external signals (input) from the subject body (output) [17].

3.1. Power block

Following the above mentioned recommendations, the ESB is powered by a single 9 V battery and a voltage regulator (U5) provides a stabilized 5 V to the circuit. The capacitors C6, C7, C8 filter the 50–60 Hz power line noise, while the red LED (D2) and the limit resistor R6 serve as a visual indicator for the ON/OFF power switch SW3.

3.2. Isolation block

Electrical isolation is obtained by a 4N35 optoisolator (U3), whose pull-down resistor is R7. The isolation block supports an input voltage range of $V_{IN} = \pm 20$ V, limited by the diode D2 and the resistor R1, while the minimum voltage to turn on the input side is $V_{IN}^{min} \approx +1.5$ V. It provides an electrical isolation up to 5 kV_{RMS}.

3.3. Trigger block

The output side of the optoisolator is fed into the not-inverting input of an operational amplifier (OPAMP) U2, while the inverting input is set at a 2.5 V by means of a voltage divider (R11 and R12). Since U2 is set in open-loop configuration, it behaves as a comparator [18] with a fixed threshold voltage of 2.5 V. The swtitch SW2A/B changes the comparator's functioning: position 1–4 set the comparator high (i.e. at +5 V) when the optoisolated signal is greater than the threshold (namely, 1 High), while position 3–6 set the comparator high when the optoisolated signal is lower than the threshold (namely, 1 Low).

3.4. Timer block

The output of the trigger block is connected to the timer block, based on a NE555 (U3) in a monostable multivibrator configuration. Regardless of the input trigger duration, this guarantees an output pulse with a minimum width given by [18]:

$$T_{min} \approx 1.10 R_3 C_4 \approx 3.63\ ms \tag{1}$$

By limiting the pulse width, unstable properties of the SYNC, such as the bouncing phenomena produced by response buttons, is avoided. Additionally, the minimum threshold on the pulse duration guarantee that even short SYNCs are still detectable at low sample frequencies (e.g. lower than 300 Hz).

NE555 gives a pulse amplitude of 3.65 V, about 70% of the 5 V power level. The capacitor C1, placed between PIN5 and ground, filters the 50–60 Hz power line noise. The output of U3 is connected to the LED D1 (R2 is LED's limiting resistor) that provides a visual feedback of each generated pulse. Additionally, U3 drives the dedicated TTL outputs, 4 3.5 mm mono jack connector (J2–J5) with signal and ground connected, respectively, to the tips and the sleeves. Timer's output can sink/source up to 200 mA. Considering that the input current of a TTL ports do not typically exceeds ±1 mA [19], 4 different TTL inputs can be simultaneously driven.

3.5. Filter block

A periodic square wave, as well as an a-periodic pulse signal, with a non-ideal rise time $t_r > 0$ concentrates most of its spectral energy at $f_K < 0.5/t_r$ [20]. This can generate cross-talk effects due to inductive or capacitive coupling, expecially in low-speed circuits where parasistic capacitances and inductances are not minimised. A solution to mitigate the cross-talk effect is to lower f_k, namely slowing the rise times. Accordingly, the output of the timer block is filtered with a passive first-order RC (low-pass) filter, whose cut-off frequency is given by [21]:

$$f_c = 1/(2\pi R_8 C_3) \approx 1591\ Hz \tag{2}$$

The filter block finally drives 4 voltage buffers (U1A–U1D), that provides 4 analog (i.e. filtered pulses) outputs: three (U1B–U1D) in the range 0–3.65 V, while one (U1A) in the range 0–3.65 mV, by means of a voltage divider (R4 and R5). Similarly to the TTL ones, the analog outputs are wired to four 3.5 mm mono jack, with signal and ground connected, respectively, to the tips and the sleeves.

3.6. Connection cables

In order to reduce the external noise, we recommend the use of a 2-conductor shielded and twisted cable to connect any external device to the analog and TTL outputs of the ESB. The shield reduces the electrically-coupled noise, while the twisting configuration cancels the magnetically-coupled noise. To prevent unwanted ground loops, the shield must be connected to the ground at the output side only, while is left floating to the other side [22].

4. Design files

Design Files Summary

Design filename	File type	Open source license	Location of the file
Electronic schematics	Kikad *.sch file, *.pdf file	GNU General Public License (GPL) 2.0	https://osf.io/ctkmh https://github.com/mbilucaglia/ESB
PCB layout	*.grb file	GNU General Public License (GPL) 2.0	https://osf.io/ctkmh https://github.com/mbilucaglia/ESB

5. Bill of materials

A complete bill of materials, including supplier's Part ID of each component, is available as a spreadsheet file in the article's repositories (https://osf.io/ctkmh,https://github.com/mbilucaglia/ESB). The price of the components is in the author's local currency (Euros), as provided by the supplier's regional location (Italy).

6. Build instructions

Some soldering skills are required to build the ESB. The components (all in through-hole technology) can be easily mounted on protoboard using a point-to-point wiring (see Fig. 2). For ease of assembly, we suggest a protoboard large at least 4×4, but smaller sizes are possible.

Component soldering does not present particular difficulties. The only recommendation that we give is to connect the female jack connectors, the pus-pull button, the LED and the switches to the protoboard using wires long at least 20 cm, in order to allow them to be permanently mounted on the top cover (using e.g. glue gun for the jack connectors and the LEDs, as well as the provided bolts for the switches) without limiting the box opening.

The wires can be permanently soldered to the protoboard or connected using female-male strips, cut (from the available 20 pins ones) in 3 different sizes:

- qt.2–8 pins connectors for the analog (P6) and the TTL outputs (P7);
- qt.4–2 pins connectors for the switches (P4), the button (P2), the LEDs (P5, P8) and the analog input (P1);
- qt.1–4 pins connector for the switch (P3).

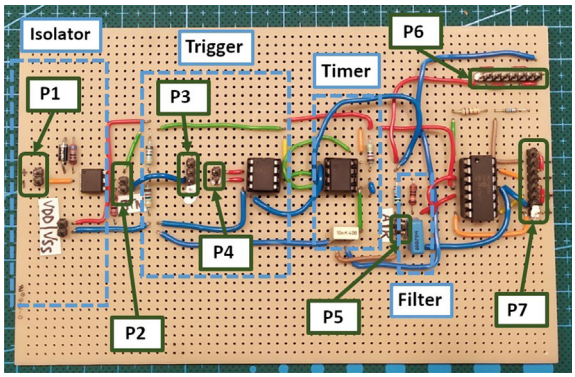

Fig. 2. Internal layout (circuit mounted on a protoboard) of the ESB.

The power block of the ESB (i.e. SW3, D2, R6, C8, U5, C6, C7) can be mounted on a separated smaller (e.g. 1×1.5) protoboard, since it is connected to the rest of the ESB circuit by power wires only (see Fig. 3).

7. Operation instructions

With respect to the external layout of Fig. 4, the proper connection between the ESB and the external device requires the following steps:

1. Turn the ESB on;
2. Connect the input signal to the input connector;
3. Adjust the trigger functioning to ensure that the state LED is off when the input signal is at 0 logic level;
4. Test the input connection generating a signal at logic 1 level and ensuring that the state LED turns on;
5. Connect the output connectors to the external devices to be synchronised, according to their available synchronization inputs;
6. Test the output connections pushing the test button and ensuring that the external device is receiving a pulse.

8. Validation and characterization

The validation and characterization of the ESB was made in terms of 11 different parameters that we extracted from the technical manuals of the pre-existing commercial synchronization boxes (see Table 1). The galvanic isolation was not directly measured and the reported value was taken from the 4N35's datasheet. Similarly, the minimum pulse out duration was not measured, since it depends on the tolerances of R_3 and C_4, as explained below in the text. The input and output voltages, as well as the minimum input and output pulse duration, were measured during, respectively, static and dynamic characterization processes. The latter includes additional measures, namely the propagation delays and the maximum trigger frequency.

The static characterization of the ESB was computed using as an input signal a bench power supply (KPS305D, by Eventek) whose voltage was manually swept in the range ± 20 V. We found that the ESB supports an input range of ± 20 V and provides an output voltage swing of about 0–3.65 V (see Fig. 5). These values corresponds to the static characteristic of the TTL output, since the high input resistance (about 10 $T\Omega$) of voltage buffers provides only a negligible attenuation when partitioned with the R8 resistor. The logic 1 and 0 at 0 V and 3.65 V, respectively, is fully compatible with the standard TTL thresholds, as well as the transition voltage at approximately 1.7 V [19].

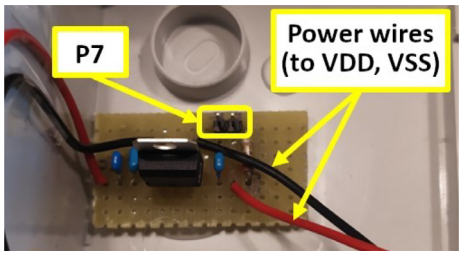

Fig. 3. Internal layout (circuit mounted on a separated protoboard) of the power block.

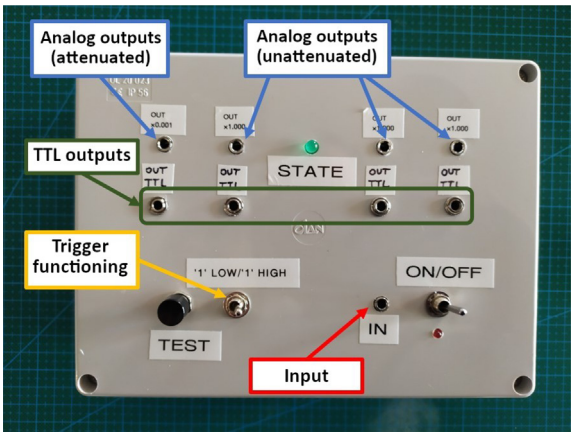

Fig. 4. External layout (top panel of the enclosure box) of the ESB.

The dynamic characterization of the ESB was computed using a 9350C oscilloscope (Le Croy) and a UDB1002S signal generator (Sain Smart). A 0–5 V square waveform, generated by the UDB1002, was used as a pulse-like input signal, while the output (either TTL or analog) was simultaneously measured by the 9350C, as shown in the Fig. 6. The pulse-width (*PW*) of a square wave with a frequency *f* and the duty-cycle *DT* is given by:

$$PW = DT/f \tag{3}$$

The minimum input pulse duration is defined as the smallest pulse width of an input signal that guarantees an output pulse with a nominal (i.e. 3.63 ms) pulse width. It was measured by linearly varying the pulse width of the test signal according to Eq. (3) and simultaneously measuring the output pulse width. Due to a limitation of the used signal generator, we were able to decrease the input pulse duration to a value as low as 50 µs, still guaranteeing a 3.63 ms-long output pulse.

The minimum trigger period is defined as the minimum temporal distance between adjacent input pulses that produces distinguishable output pulses. It was measured by varying, according to Eq. (3), the period of the input signal with a fixed 50 µs-long pulse-width and by simultaneously counting the number of output periods. We found a minimum trigger period of 5 ms, corresponding to a maximum trigger frequency of 200 Hz.

As described in Eq. (1), the minimum output pulse width depends on R_3 and C_4. Accordingly, variations of resistance and capacitance values from the corresponding nominal values produce a variation of the pulse width. Let ϵ_{R_3} and ϵ_{C_4} be the tolerances (expressed in percentages of the nominal values) of, respectively, R_3 and C_4. Assuming ϵ_{R_3} and ϵ_{C_4} "small", the tolerance (expressed in percentage of the nominal value) of the output pulse-width ϵ_T is given by: [23]:

$$\epsilon_T \approx \epsilon_{R_3} + \epsilon_{C_4} \tag{4}$$

Following Eq. (4), a 1% tolerance on R_3 and a 10% tolerance on C_4 gives $\approx 10.05\%$ tolerance on the output pulse-width, namely 3.63 ± 0.381 ms.

The propagation delay is defined as the temporal distance between the mid points (i.e. 50% of the maximum level) of the input and output signals in the rising transition (i.e. $1 \rightarrow 0$). The input signal consisted in 256 0–5 V pulses with a fixed pulse width of 50 µs and a period of 50 ms, corresponding to 10 times the minimum trigger period. For each pulse, the temporal distance between the input and the output was independently measured. The TTL output showed a propagation delay of

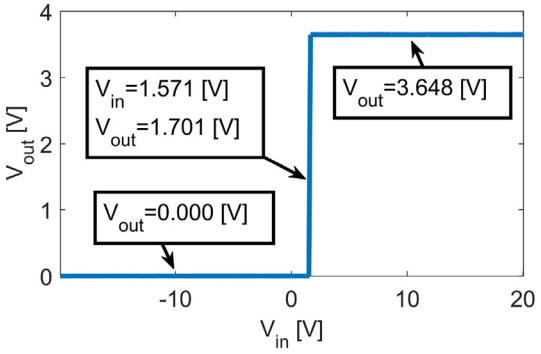

Fig. 5. Static characteristic of the ESB.

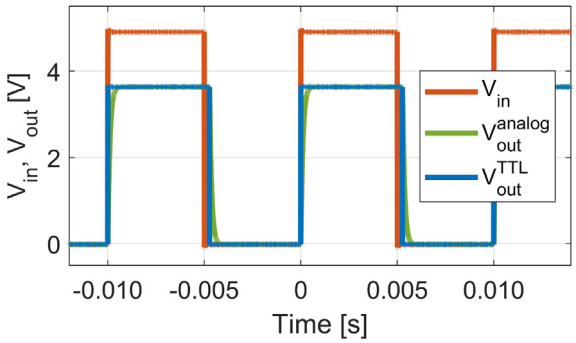

Fig. 6. Input and output (analog and TTL) signals.

Table 2
Statistics of the propagation delays for the TTL and analog outputs ($N = 256$ measures).

Output	Mean	Std. Dev.	Min	Max	Q1	Q2	Q3
TTL	3.354 µs	0.001 µs	3.334 µs	3.410 µs	3.348 µs	3.351 µs	3.354 µs
Analog	74.209 µs	0.290 µs	373.241 µs	74.935 µs	73.997 µs	74.241 µs	74.410 µs

3.354 ± 0.001 µs, while the analog un-attenuated output showed a propagation delay of 74.209 ± 0.290 µs. The following Table 2 reports the statistics (mean value, standard deviation, minimum value, maximum value, first quartile, second quartile and third quartile) of both the TTL and analog propagation delays.

9. Conclusions

In this paper, we described a EEG Synchronization Box (ESB), a cost-effective solution to send a SYNC signal to 8 different EEG devices, both analog and TTL-compatible. ESB can be used in situations where a precise temporal alignment is required, such as ERP and ERD/ERS experiments, hyperscanning setups and EEG-fMRI studies. The ESB assembly does not present particular difficulties: the components can be soldered on a protoboard using point-to-point wiring.

When compared with pre-existing commercial synchronization boxes (see Table 3), ESB showed the largest input voltage range (±20 V), the shortest minimum output pulse duration (3.3 ms), the largest galvanic isolation (5 kV) and a selectable trigger functioning mode. The fixed threshold voltage makes ESB less flexible: additional amplification and/or level shifter blocks are required in order to generate the appropriate input signal when using, e.g. microphones and light sensors. ESB has the lowest number of inputs, but the only one that allows multiple outputs. The minimum input pulse duration seems to be the largest, but it should be repeated that during the characterization steps we were able to decrease the input pulse duration to a value as low as 50 µs, due to a limitation of the signal generation: we expect a lower effective minimum input pulse duration, at microsecond scale. Finally, the price of the ESB is the lowest, about two orders of magnitude smaller that the others.

The additional measures of propagation delay and maximum trigger frequency cannot be considered in a comparative evaluation, since they are not indicated in the pre-existing commercial devices. We showed that ESB can distribute up to 200 SYNC pulses per seconds, with a delay of 3.354 ± 0.001 µs and 74.209 ± 0.290 µs for, respectively, the TTL for the analog outputs.

Table 3
Comparison between ESB and some pre-existing commercial synchronization boxes.

	StimTrack (Brain Products)	g.TRIGbox (g.TEC)	ESB
Input voltage	±5 V	±0.5 mV ±200 mV ±100 mV ±5 V	±20 V
Treshold voltage	adjustable	adjustable	fixed (1.7 V)
Output voltage	±5 V (analog) 0–5 V (TTL)	0–200 mV (analog) 0–5 V (TTL)	0–3.3 V (analog) 0–3.3 mV (analog) 0–3.3 V (TTL)
Galvanic isolation	1.5 kV	4 kV	5 kV
Trigger modality	1 High	1 High	1 High or 0 High
Minimun pulse in duration	10 µs	N/A	50 µs
Minimum pulse out duration	11 ms	20 ms	3.3 ms
#Inputs	1	4	1
#Outputs	1	4	8
Indicative price	1300.00 €	2900.00 €	35.00 €

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Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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